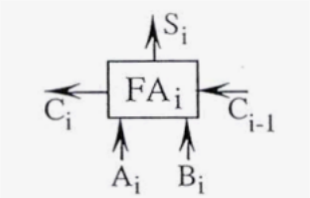
Problem 1 (Number systems and Ripple-carry adder) (5 points)

The full adder can be denoted as a module as shown below:



(a) Draw the block diagram of an **8-bit ripple-carry** adder using the above module as building blocks. The adder should be able to perform the **add/subtract** operations under the control of a signal K in the following way:

when $K = 0$, $S = A + B$

when $K = 1$, $S = A - B$

where $A = A_7A_6...A_1A_0$, $B = B_7B_6...B_1B_0$, $S = S_7S_6...S_1S_0$, all in two's complement representation. You should add to your diagram a **minimum number** of extra gates to output the four statuses, N, V, Z, and C as defined in Problem 2, Lab. 2.

(b) Given two decimal integer numbers in sign-magnitude representation:

$A = -90$ $B = -128$

Convert them into 8-bit equivalent binary integer numbers in two's complement representation, and then simulate the computer to perform the operations A+B and A-B to produce the results S, N, V, Z, and C.

(c) Some computers provide two special operations (see below) in their instruction sets and control them by a control signal K so that

when K = 0, $S = A + B + C_{in}$ — called "add with carry" operation;

when K = 1, $S = A - B - C_{in}$ — called "subtract with borrow" operation;

where C_{in} is a given external carry/borrow signal participating in the regular add/subtract operation. Each of the above operations must be executed in its entirety in only one clock cycle.

You are required to modify the circuit in Part (a) for accommodating these two special operations. Give the **design procedure** and draw only the modified part of your diagram.

(d) Assuming $C_{in} = 1$, use the same data A and B obtained in Part (b) to perform the two special operations specified in Part (c) on your designed adder. Give the results of S, N, V, Z, and C for each operation.

Problem 2 (Full-adder circuit and Hazard analysis) (5 points)

(a) In Lab 2, Problem 1, you have created an **XNOR-based** full adder circuit consisting of two XNOR gates and three NOR gates. Draw this circuit and give the names A_i, B_i, C_{i-1} and S_i, C_i to its inputs and outputs, respectively.

(b) Assume that every gate has a delay of one time unit. Analyze the above circuit to find its dynamic behavior at the input transition $A_iB_iC_{i-1} = 111$ to 100. You should trace the circuit, gate by gate, in order to **detect the hazard**, draw the **waveforms for** S_i **and** C_i for the given input transition, and **find the amount of delay** (in time units) for each of S_i and C_i.

(c) Repeat Part (b) for the input transition $A_iB_iC_{i-1}$ = **001 to 100.** Based on the results of these two analyses, can you predict more (at least, two, but could be many) other cases which will cause hazards?

Problem 3 (Design of Combinational Circuit) (5 points)

Given the problem specification as follows:

"A four-variable combinational function, F(A,B,C,D), equals to 1 iff only 3 or 2 of its independent **variables equal to 1, otherwise the** function value equals to 0."

(a) Write the truth table.

(b) Write the canonical sum-of-products expression for the given function. Use any method to convert it into a simplest expression such that it can be implemented with only **3 XOR** and **4 AND** or **OR** gates. No inverted input variables are available. Give your **design procedure** and derive the expression.

(c) Draw the circuit diagram.

Problem 4 (Multiplexer) (5 points)

(a) Implement the function given in Problem 3 using only one 8x1 multiplexer and one inverter. Give your design procedure and draw the block diagram.

Note: The internal circuit of the multiplexer is not required. Same for part (b).

(b) Using the same method of design, show that with only three additional gates selected from AND, OR, and NOT you can build the same function in Problem 3 on only one 4x1 multiplexer. Give the design procedure and draw the block diagram.